



# Silicon Substrate for RF –CMOS Applications

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## Abstract

Dielectric substrate selection plays important role at RF frequencies due to confinement of energy and its impact on the overall loss. The substrate permittivity which correlates with the energy storage significantly affects the circuit performance at higher frequencies. The substrates are segregated into lossy dielectric or good dielectric according to the permittivity behavior. The loss tangent value depends on the permittivity and affects the quality factor of the transmission line. In silicon the metal contact give rise to the Schottky contact due to metal- semiconductor junction. This necessitates proper formulation and modeling to be carried out for predicting circuit behavior. Various phenomena such as doping, carrier mobility, frequency is the major contributing factor effecting the permittivity and their role on loss tangent are studied and detailed in this article

**Keywords:** Substrate; Complex Permittivity; Silicon; Resistivity

## Introduction

Silicon with finite resistivity behaves differently at RF frequencies compared to generic substrate considered as a good dielectric such as alumina, RT-Duroid, FR4. Lossy as well as good dielectric material can be characterized by complex permittivity. Silicon which is considered as the lossy substrate also have considerable amount of dissipative energy associated with the complex permittivity. Permittivity is the property of the dielectric which indicates capacitance or stored charges mathematically associated with the imaginary part. The loss tangent can be deduced with the current density which in turn depends on complex permittivity. Material permittivity relates with the physical phenomena and main contributors are ionic conduction, dipole friction, and dipolar relaxation, atomic and electronic polarization [1]. Real part of the complex permittivity remains constant up to microwaves but reduces at millimeter wave region whereas imaginary part increases in this region and it can be attributed to dipole relaxation whereas in infrared region the atomic and electronic polarization causes the absorption peaks resulting in more losses at higher frequencies. The effects are more prominent by the applied electric field as nucleus displace with respect to surrounding electrons in the case of electric polarization whereas in case of atomic polarization positive and negative segregation for ions higher permittivity materials particularly at higher frequencies.

Silicon as semiconductor is considered as a lossy substrate due to its finite resistivity [2]. The effect of lossy substrate on circuit performance is unpredictable and leads to higher losses

leading to dissipative current [3]. This effect is primarily due to the higher bounded charges and reflects in the higher imaginary part of the permittivity which increases with the frequency. The micro strip configuration with metal- semiconductor leads to Schottky junction and the transmission line model to be modified due to this phenomenon. This necessitates proper modeling of the silicon substrate for predicting the behavior at RF frequencies [4]. Transmission line on silicon behaves as diode rather than pure conductive line and commonly employed planar transmission line is micro strip [5,6]. Micro strip structure consists of the metalized top and bottom surface in which silicon acts as a dielectric layer between two conducting surfaces. The behavior of silicon varies as it consists of both free and bounded charges which varies with frequency. Further metal contact with the semi-conductor leads to Schottky behavior and having conduction as well as displacement current density. The resistivity of silicon can be further changed with the doping which is standard microelectronics process [7]. This necessitates modeling to predict behavior due to the various phenomena associated with the variable capacitance and resistance. The article details various factor impacting RF losses and permittivity in the silicon particularly due to resistivity, interfacial layer stacking, and frequency and discusses the associated phenomena.

## Complex Permittivity

Permittivity is related with the charge retention capacity of the medium so higher dielectric constant  $\epsilon$ , generally leads to more

heat. In dielectric materials with the application of external bias the bound charges are displaced which creates dipole field that opposes the applied electric field E causing polarization of the atoms or molecules of the material [5]. Relation between displacement flux D, electric field E and polarization P can be represented as

$$D = \epsilon_0 E + P \text{ (Electric polarization)}$$

$$P = \epsilon_0 \chi_e E; \chi_e \text{ Electric susceptibility}$$

$$D = \epsilon_0 E + \epsilon_0 \chi_e E = \epsilon_0 (1 + \chi_e) E = \epsilon_0 \epsilon_r E = (\epsilon' - j\epsilon'') E$$

The relative permittivity can be expressed as

$$\epsilon_r = \frac{\epsilon' - j\epsilon''}{\epsilon_0} = \epsilon_r' - j\epsilon_r'' = \epsilon_r' (1 - j \tan \delta)$$

In case of semiconductor, charges are free and bounded which contributes the current by applying electric field. The concept of permittivity can be deduced from the Maxwell's equation

$$\tan \delta = \frac{\omega \epsilon'' + \sigma}{\omega \epsilon'} \approx \frac{\epsilon''}{\epsilon'} \dots \dots \dots (1)$$

$$Q = \frac{1}{\tan \delta} = \frac{\omega \epsilon'}{\omega \epsilon'' + \sigma}$$

The imaginary part associated with the permittivity accounts for losses in the medium due to damping of the vibrating dipole moment [7,8]. Dielectric loss due to damping effect can be further correlated with electric susceptibility and higher susceptibility renders more heating. In the case of semiconductor  $\sigma = q\mu n$  so for frequency 'f' using eq (1)

$$\tan \delta = \frac{(\omega \epsilon'' + q\mu n)}{\omega \epsilon'} = \frac{G}{\omega C} = \frac{\text{conduc} \tan ce}{\text{capaci} \tan ce}$$

$$\omega = 2\pi f$$

The generalized conductivity can be represented as

$$\sigma = nq\mu_n + pq\mu_p \approx nq\mu_n$$

In case of microstrip line mostly for narrow lines [9], the relative permittivity can be represented as

$$\epsilon_r = \frac{C_d}{C_a} = \frac{c}{v_p^2} = \frac{\text{velocity.of...light}}{\text{Phase.velocity}}$$

where c is the velocity of light, Ca is air capacitance, Cd is the dielectric capacitance. Variation of tanδ with frequency is more prominent compared to ε<sub>r</sub> at microwave ranges. Lossy dielectric such as silicon having higher dielectric susceptibility leads to more polarization. The losses in the dielectric can be represented by generic term of power factor which represents power factor of condenser containing the dielectric

Power factor =  $\cos(90^\circ - \delta) = \frac{\epsilon'}{\sqrt{(\epsilon')^2 + (\epsilon'')^2}}$ ; It can be equated to tan δ for  $\epsilon' \ll \epsilon''$ ,

Permittivity of any material can't be lesser than ε<sub>0</sub> and classification of perfect dielectric, good dielectric and lossy dielectric can be represented in RF ranges [10] as shown in Table 1. Generally, in case of pure semiconductor, dissipation factor is taken as ~1 which indicated conduction current density equals to the displacement current density ( $J_c = J_d; \sigma = \omega \epsilon$ ). Silicon substrate is considered neither a good conductor nor a good dielectric due to finite conductivity and resistivity. Losses in the silicon can be varied by the resistivity variation. In the case of silicon, contribution of

the metallic losses is not affected by the substrate resistivity for microstrip configuration and major loss contributions are from dielectric as well as due to surface wave propagation in silicon substrate.

**Table 1:** Classification of dielectric material in terms of permittivity.

Dielectric	Permittivity behavior
Perfect	$\epsilon'' = 0$
Good	$\epsilon'$ remains constant, $\epsilon''$ considerably small and increase with frequency
Lossy	Both $\epsilon'$ and $\epsilon''$ varies with frequency

### Concept Of Loss Tangent

Substrate permittivity affects the conductor, dielectric, and radiation loss in the microstrip line. All these mechanisms are dependent on the substrate permittivity resulting in various phenomena such as surface wave, ground wave, leaky wave or radiated wave. Selection of dielectric is very important as substrate with high dielectric constant can introduce losses. It also governs the width, propagation characteristics, line length, losses, and various modes of propagation. Generally dielectric loss is less compared to conductor losses in microwave region, but for lossy substrate such as silicon the effect is considerably high and affects the circuit performance considerably at higher frequencies. Dielectric loss represented by the loss angle (eq 1) can also be represented as:

$$\tan \delta = \frac{\omega \epsilon'' + \sigma}{\omega \epsilon'} = \tan \delta_d + \tan \delta_L \dots \dots \dots (4)$$

In general case the term  $\tan \delta_L$  is negligible and only contributing factor is from  $\tan \delta_d$ . The first term  $\tan \delta_d$  resulted from the polarization loss associated with intrinsic substrate and second term  $\tan \delta_L$  is defined as extrinsic loss resulted from the finite conductivity of the substrate which is applicable for silicon [3]. Various other factors such as temperature and humidity also impact the dielectric constant value. The dielectric loss (for narrow lines) can also be represented as [11].

$$\alpha_d = \frac{\sigma}{2} \sqrt{\frac{\mu}{\epsilon}} = 1.634 \times 10^3 \frac{\sigma}{\epsilon_r} \text{ dB/cm}$$

Dielectric loss due to damping effect can be further correlated with electric susceptibility as higher susceptibility renders more heating. Various factors effecting the dielectric loss tangent are detailed as below:

### Effect of Frequency

The increase in the frequency results in the increased losses in semi-conductor compared to alumina substrate as ε' remains constant but ε'' varies with frequency, so variation in tan δ is observed as shown in Table 2. Other substrates such as TFG also demonstrate the above-mentioned effect [12].

**Table 2:** Frequency effect on the dielectric loss.

Material	Frequency (GHz)	tan δ
Silicon (higher resistivity)	1	0.005
	10	0.015
Vaseline	0.1	0.00004
	3	0.00066
Water	0.001	0.04
	3	0.157
Alumina	1	0.0002
	10	0.0003

**Effect of Impurity**

In case of alumina substrate, tan δ value varies with purity level and highest purity (99.5%) yields lowest loss tangent. The increase in purity from 96% to 99.5% can change the loss tangent by 3 times. This also relates with the doping concentration as increase in impurity level increases loss tangent (Table 3).

**Table 3:** Impurity effect on dielectric loss.

Impurity concentration	tan δ	Value increment
0.5% (99.5%)	~0.0002	-
3.50%	~0.0006	3 times
14.50%	~0.0015 (15 times)	15 times

**Effect of Resistivity**

**Table 4:** Substrate resistivity effect on dielectric loss.

Resistivity	tan δ
Silicon (1-10 Ω -cm)	~0.01
Silicon (~1 k Ω -cm)	~0.001
Silicon (~10 k Ω -cm)	~0.0001

The semiconductor substrate silicon also shows loss behavior varied with the change in resistivity. Table 4 shows that an order of increase in resistivity decreases the losses [13]. The above relation clearly shows that resistivity plays important role in the dielectric loss and can be correlated with the recombination time τ as

$$\sigma = q\mu n$$

$$q = I_d \tau$$

$$\sigma = I_d \tau \mu n \dots \dots \dots (2)$$

where Id is the stored charge current and is the recombination lifetime. High permittivity substrates are good at holding charges where low permittivity material having low ability to polarization and holding charges Substrate losses for silicon in case of 10k Ω -c-m are 0.032 dB/cm which increases to 32 dB/cm for the resistivity of 10 ohm-cm. High resistivity silicon substrate (1 k Ω -cm)

is having attenuation of the order of 10<sup>-3</sup> compared to 10<sup>-4</sup> for silicon with resistivity of 10 k Ω -cm. The cut off frequency phenomena can be written as

$$f_T = \frac{1}{2\pi\tau} = \frac{\sigma}{2\pi\epsilon} = \frac{1}{2\pi\rho\epsilon} \dots \dots \dots (3)$$

Free charge carriers cause the main part of the losses in the semiconductor and as seen from equation (3), the main loss contribution is due to finite conductivity. At lower end of the frequency, real permittivity remains constant and the cut off frequency is dependent on the substrate resistivity. In semiconductor, the doping phenomena to be correlated with the change in resistivity and losses further increases as doping reduces the carrier mobility.

**Transmission Line Modelling**

The metal on the semiconductor material silicon results in the Schottky junction [7]. Schottky diode is having both resistance and capacitance non-linearity. The semiconductor with Schottky barrier contact can be represented as capacitance and un-depleted region as resistor. The resulting equivalent circuit is the combination of non-linear capacitance and resistance. The resistance value also varies at higher frequencies as the current through the non-depleted region can crowd to the outside edge of the material due to the skin effect [14] and thus increasing the resistance.

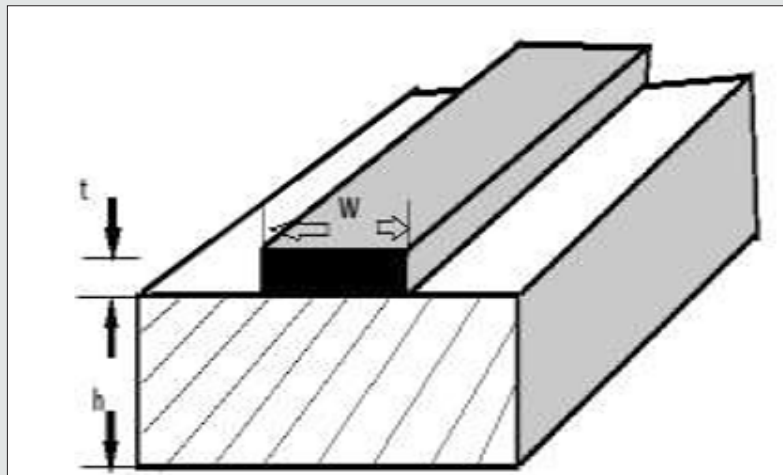
$$C(V) = \frac{C_p}{\sqrt{\phi_{bi} + V_{bias}}}; Q(V) = \sqrt{a(\phi_{bi} - V)}$$

where c<sub>p</sub> is the capacitance at zero bias voltage, a is constant and V is the applied voltage. The stored charges can be represented as: Q(V)=a<sub>0</sub>+a<sub>1</sub>V+a<sub>2</sub>V<sup>2</sup>+a<sub>3</sub>V<sup>3</sup>+.... And I (t)= dQ/dt= [ a<sub>1</sub>+2a<sub>2</sub>V+3a<sub>3</sub>V<sup>2</sup>+....] (dV/dt); where V=V<sub>0</sub> sin ωt. The equivalent model of microstrip on silicon can be shown in the (Figure 1a). The conductance G and variable capacitance (C) is accounted due to Schottky contact. The total current density in the non-depleted region can be shown as in (Figure 1b). The change in depletion layer width with the doping changes the current density. Further increase in frequency results in charge deposition which can change the resistance value in the un-depleted region [15]. The resultant phenomena shown in Table 5 summarizing the effect of various parameters on the various device aspects. Time varying electric field induces conduction and displacement current. Polarization dipoles having finite mass moves back and forth with the frequency resulting in the delayed response and at higher frequencies, polarization vector lags behind the applied electric field. The relaxation time representing charge density decay can be represented as

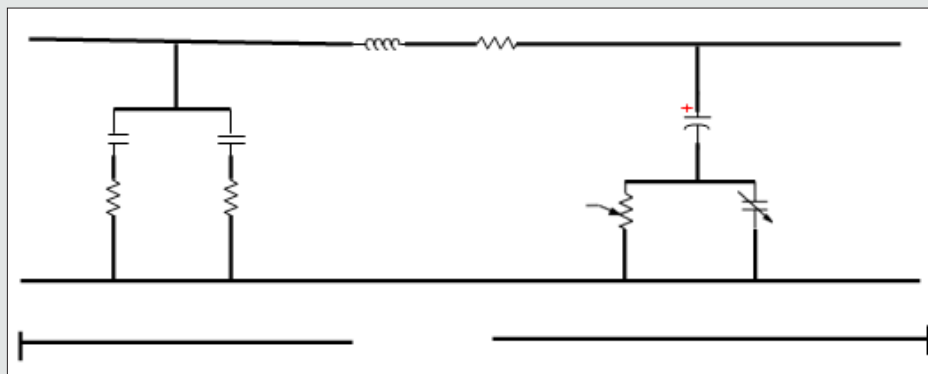
$$J = (q\mu n + \omega\epsilon'' + j\omega\epsilon')E$$

$$E = \frac{V}{d}$$

$$Q = \frac{1}{\tan \delta} = \frac{\omega\epsilon'}{\omega\epsilon'' + \sigma} = \frac{\omega C}{G} = 1/D$$



**Figure 1a:** Microstrip transmission line for Silicon accounted due to Schottky contact. The total current density in the non-depleted region can be shown as in Figure 1b.



**Figure 1b:** Conductance & capacitance due to Schottky.

**Table 5:** Effect of various parameters on the device.

Parameter	Current density	Breakdown voltage	Loss
Doping ↑	↑	↓	↑
Frequency ↑	↑	-	↑
Temperature ↑	↓	-	↑

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the applied electric field. The relaxation time representing charge density decay can be represented as

$$\tau = \frac{\epsilon}{\sigma} = \frac{\epsilon}{\rho\mu}$$

The delay changes with the resistivity and at higher resistivity the delay reduce as per the equation. An order increase in the resistivity decreases approximately an order in the relaxation time. This delay is important for the charge depletion effect in the substrate and Table 6 shows delay associated with some common semiconductor materials. Permittivity value is also affected with the temperature and humidity as the mobility of charge carriers decreases with the temperature due to lattice scattering. The effect of temperature on the permittivity is shown in Table 7. Silicon substrate is deposited with the thin layer of oxide before initiating further processing [16]. So, for silicon substrate, the losses are primarily from substrate and interface losses induced between the insulation layer and silicon substrate. These losses can be minimized by employing high quality gate oxide in conjunction

with high resistivity silicon substrate (Figure 2). The compound semiconductor permittivity depends on the thickness of individual material (taking  $t_1$  and  $t_2$ ) and as shown in the below figure the role of substrate thickness plays important role after certain layer thickness. Compared to 25mils thick substrate in case of lesser substrate thickness (10mils), the permittivity variation is more prominent with oxide or nitride over the silicon substrate mostly attributed to the higher field penetration (Figures 3a & 3b).

The effective permittivity can be shown as

$$\frac{t}{\epsilon_{eq}} = \frac{t_1}{\epsilon_1} + \frac{t_2}{\epsilon_2} \dots\dots\dots (4)$$

$$\epsilon_{eq} = \frac{t(\epsilon_1\epsilon_2)}{t_1\epsilon_2 + t_2\epsilon_1}$$

Table 6: Relaxation time.

Material	$\tau$ minority (sec)
Si (std resistivity)	$2.5 \times 10^{-3}$
GaAs	$\sim 10^{-8}$

Table 7: Temp dependent phenomena in semiconductor.

Temperature (K)	Dielectric constant
100	$\sim 11.5$
200	$\sim 11.7$
300	$\sim 11.8$
400	$\sim 12.0$
500	$\sim 12.1$
600	$\sim 12.3$

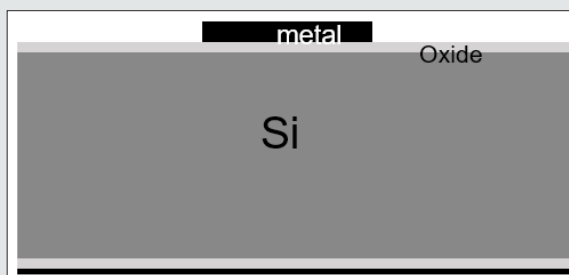


Figure 2: Microstrip line over thin layer of oxide.

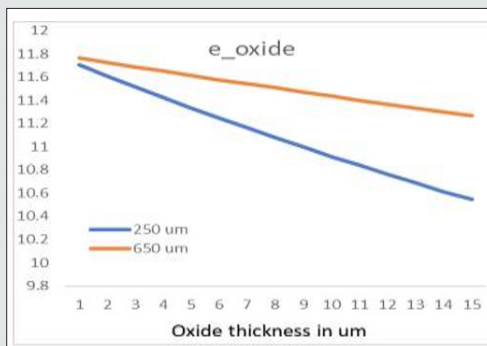


Figure 3a: Effective permittivity due to interfacial of Oxide interfacial layer.

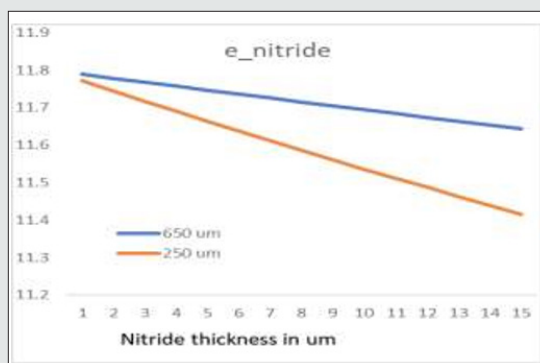


Figure 3b: Effective permittivity due to interfacial of Nitride interfacial layer.

The above formula (eq 4) considers the ideal substrate but in case of silicon apart from the permittivity the losses associated with the finite resistivity of the substrate is not considered. Higher thickness of layer is needed in case of low frequency and the same can be minimized at higher frequencies as the effective permittivity is minimally varied. Further the quality of oxide or nitride deposition either by PECVD or LPCVD has minimal role in

the RF circuit performance. Interface layer of oxide and nitride are most commonly used [oxide (500 Å) and nitride (1500 Å)]. The effect of these layers on the effective permittivity and attenuation is shown as below in Figure 4. The experimental study conducted as shown in (Figure 5a & 5b) shows that surface defects associated with the bare silicon plays important role in the overall losses at higher frequencies.”

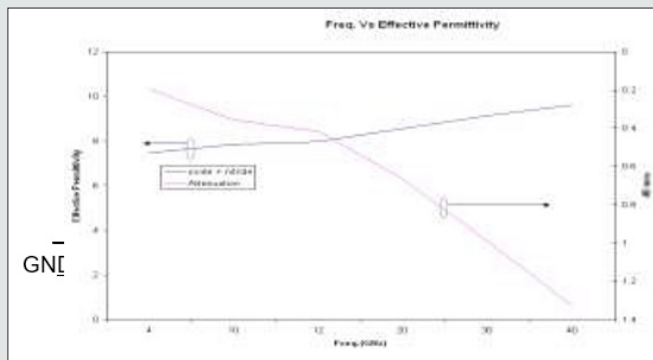


Figure 4: Effect of interfacial layer on the losses.

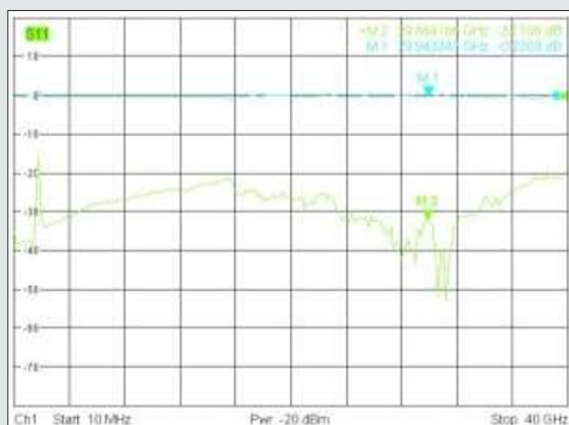


Figure 5a: Effect of interfacial layer on the losses with oxide layer.

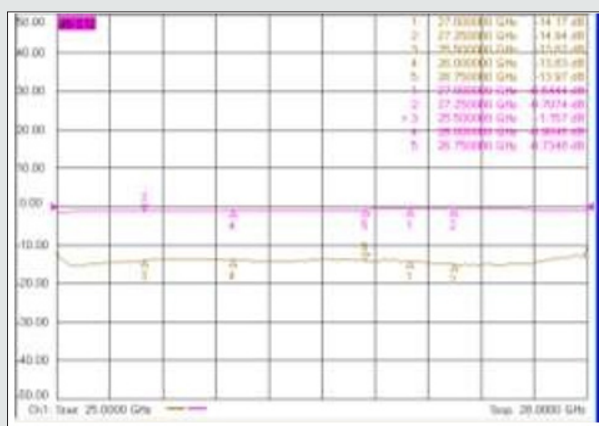


Figure 5b: Effect of interfacial layer on the losses without oxide layer.

## Conclusion

Silicon has become intrinsic part of semiconductor industry and implementation of RF-CMOS becoming reality. This necessitates the understanding of silicon as a dielectric at higher frequencies so as to accurately predict the circuit realization on silicon substrate. This article details the role of permittivity and its physical interpretation in context of semiconductor material especially silicon. The various phenomena affecting the overall permittivity is presented considering isotropic material. Role of doping, impurity, temperature on the permittivity along with quality factor and loss tangent is also detailed. The correlation presented in the article shows that increase in frequency and doping result in the increase of the losses which are associated with the loss tangent. The concept of doping which is standard process in microelectronics results in the resistivity variation. This also results in the increase in current density while decreasing breakdown voltages. As metal over the semiconductor substrate creates Schottky contact so accurate modeling can predict the circuit behavior. Major outcome of this study is: Relaxation time associated with the substrate resistivity which in turn effects the RF performance Field penetration effect can be minimized by choosing appropriate interfacial layer thickness. The article brings the overview of the permittivity and various phenomena associated with it particularly on silicon substrate which will help in predicting accurately behavior of circuits at higher frequencies and same study can be extended on various other semiconductor substrates. RF-CMOS structure can be implemented with the selective interfacial approach leading for the optimum performance of the structure.

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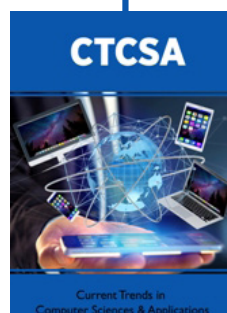
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